Claims 1-23 are currently pending and under consideration, Claims 1, 6, and 23 having been amended by way of the present amendment, without the introduction of new matter (see the specification page 34, lines 1-17 and figures 1-3).

In the present Office Action, Claims 1, 6, and 23 were rejected under 35 U.S.C. §102(e) as being unpatentable over Saito (U.S. 6,100,570). This rejection is respectfully traversed.

Turning first to Claims 1 and 23, these claims as amended each include the new limitation "said semiconductor region doped with impurities of the same conductivity type as said at least one of said plurality of device formation regions and said body region"as well as the amended limitation "wherein at least part of said at least one isolation region includes a partial isolation region having a partial insulation region formed in an upper part thereof and a semiconductor region formed in a lower part thereof *between at least two of said device formation regions*." Support for this amendment can be found in the specification, page 34, lines 8-13.

Saito fails to show a partial isolation region comprising a partial insulation region formed on a doped semiconductor region between device formation regions as claimed in pending Claims 1 and 23. For example, referring to Figure 7 of Saito, as asserted in the outstanding Official Action, the isolation region is identified by reference numeral 71, device formation regions are shown at 75, 73 represents an oxide layer, and 74 is the substrate. No doped semiconductor regions extend between the device formation regions in Saito, the isolation regions being directly superimposed on the oxide layer. Therefore, the structure of Saito in Figure 7 does not comprise a partial insulation region formed on a doped semiconductor region *between device formation regions*. Figure 7 of Saito is taken only by way of example, and chosen only for having been asserted in the Office Action, and the

above arguments also apply to all other Figures in Saito. Saito does not therefore teach or suggest all limitations of Claim 1 or of Claim 23. Claims 2-5 and 7-22 are dependent upon Claim 1, and therefore as Claim 1 is allowable, these claims are also allowable. It is therefore respectfully requested that the rejection of Claims 1-5 and 7-23 under 35 U.S.C. §102(e) as being unpatentable over Saito (U.S. 6,100,570) be withdrawn.

Claim 6 has been amended so as to recite that the body region is formed in the SOI layer and capable of fixing electric potential upon application of externally applied potential to the body region. Support for the amendment to Claim 6 can be found in the specification on page 34, lines 14-16 and on page 52, line 22 through page 55, line 6, and Figs. 41, 42 and 52, for example.

It is clear that Saito fails to disclose the body region as called for by amended Claim 6. An electric potential well 31 shown in Fig. 3 of Saito, which the Office Action relies on as corresponding to the body region of Claim 6, does not form the body region as recited by amended Claim 6.

Specifically, as is made clear by the proposed amendments noted above, the claimed body region is capable of fixing electric potential thereof (of the body region) upon either direct application of an externally applied potential to the body region, or indirect application of an externally applied potential to the body region via an interconnect layer or the like electrically connected to the body region. Referring to Fig. 41, which shows on example of the claimed structure, a connection region 80 corresponding to the claimed body region is capable of fixing electric potential thereof upon application of an externally applied potential to the connection region 80 via an interconnect layer 25 and a body contact 23. Also, referring to Fig. 52, which shows another example of the claimed structure, a connection

region 86 corresponding to the claimed body region is capable of fixing electric potential thereof upon direct application of an externally applied potential to the connection region 86.

Turning to the cited reference, Saito, it is apparent that the electric potential well 31 of Saito does not include a structure which allows the well 31 to fix electric potential thereof upon direct application of an externally applied potential to the well 31, or indirect application of an externally applied potential to the well 31 via an interconnect layer, a contact or the like.

Further, the electric potential well 31 of Saito is simply a potential distribution produced by an electric field, not exhibiting any physical structure. At least for this reason, Saito does not anticipate Claim 6 as amended. Therefore, it is requested that the rejection of Claim 6 under 35 U.S.C. §102(e) as unpatentable over Saito be withdrawn.

The present amendment is submitted in accordance with the provisions of 37 C.F.R. §1.116, which after final rejection permits entry of amendments placing the claims in better form for consideration on appeal. As the present amendment is believed to overcome outstanding rejections under 35 U.S.C. §102(e), it is therefore respectfully requested that 37 C.F.R. §1.116 be liberally construed, and that the present amendment be entered.

Consequently, the present application is believed to be in condition for allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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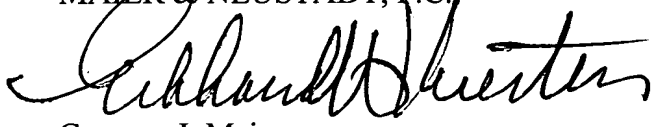

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Marked-Up Copy
Serial No: 09/466,934
Amendment Filed on:
12-14-01

IN THE CLAIMS

Please amend Claims 1, 6, and 23 as follows.

--1. (Amended) A semiconductor device having a SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, said semiconductor device comprising:

a plurality of device formation regions in which predetermined devices are to be formed respectively, said plurality of device formation regions being provided in said SOI layer;

at least one isolation region provided in said SOI layer for insulatively isolating said plurality of device formation regions from each other; and

a body region provided in said SOI layer and capable of externally fixing electric potential,

wherein at least part of said at least one isolation region includes a partial isolation region having a partial insulation region formed in an upper part thereof and a semiconductor region formed in a lower part thereof between at least two of said device formation regions, said semiconductor region serving as part of said SOI layer and being formed in contact with at least one of said plurality of device formation regions and said body region.

said semiconductor region doped with impurities of the same conductivity type as said at least one of said plurality of device formation regions and said body region.

6. (Amended) A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, said semiconductor device comprising:

a plurality of device formation regions in which predetermined devices are to be formed respectively, said plurality of device formation regions being provided in said SOI layer;

at least one isolation region provided in said SOI layer for insulatively isolating said plurality of device formation regions from each other; and

a body region formed in the SOI layer and capable of [externally] fixing electric potential upon application of an externally applied potential to said body region,

wherein said body region is formed in contact with one of top and bottom surfaces of at least one of said plurality of device formation regions.

23. (Amended) A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, said semiconductor device comprising:

a device formation region in which a predetermined device is to be formed, said device formation region being provided in said SOI layer; and

a peripheral insolation region provided in said SOI layer and surrounding said device formation region, said peripheral isolation region including a partial isolation region having a partial insulation region formed in an upper part thereof and a semiconductor region formed in a lower part thereof between at least two of said device formation regions and serving as part of said SOI layer,

wherein said semiconductor region is formed in contact with said device formation region and is floating,

said semiconductor region doped with impurities of the same conductivity type as said at least one of said plurality of device formation regions and said body region.--